Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] What is claimed is:

1. An integrated circuit design system comprising:
a second interface for displaying a plurality of description instructions corresponding to an application-specific integrated circuit (ASIC) according to a variety of display instructions;
a first interface for inputting the display instructions and for updating the description instructions displayed on the second interface according to the display instructions; and
a logic unit for updating any description instruction but an updated description updated by the first interface corresponding to the ASIC according to the updated description instruction.

[c2] 2. The integrated circuit design system of claim 1, wherein the plurality of description instructions comprises a timing slack report of the ASIC.

[c3] 3. The integrated circuit design system of claim 1, wherein the plurality of description instructions comprises a netlist of the ASIC.

[c4] 4. The integrated circuit design system of claim 1, wherein the plurality of description instructions comprises a noise analysis report of the ASIC.

[c5] 5. The integrated circuit design system of claim 1, wherein the plurality of description instructions comprises a power analysis report of the ASIC.

[c6] 6. The integrated circuit design system of claim 3, wherein the logic unit is further capable of calculating a noise analysis report corresponding to an undated netlist.

[c7] 7. The integrated circuit design system of claim 3, wherein the logic unit is further capable of calculating a power analysis report corresponding to an undated netlist.

[c8] 8. The integrated circuit design system of claim 3, wherein the logic unit is further capable of calculating a timing slack report corresponding to an undated netlist.

[c9] 9. The integrated circuit design system of claim 1, wherein the logic unit is further capable of executing a clock tree synthesis.

[c10] 10. The integrated circuit design system of claim 1, wherein the logic unit is further capable of executing a

timing optimization process.

[c11] 11. The integrated circuit design system of claim 1, wherein the logic unit is further capable of executing a cell & wire extraction process and for generating a cell & wire delay of a standard delay format (SDF).

[c12] 12. The integrated circuit design system of claim 1, wherein the second interface is capable of displaying cells and interconnects connected between the cells of the ASIC according to a specified display instruction input to the first interface.

[c13] 13. The integrated circuit design system of claim 12, wherein the second interface is capable of further displaying spare cells neighboring the cells according to the specified display instruction.

[c14] 14. The integrated circuit design system of claim 12, wherein the second interface is capable of displaying a plurality of specified icons, each of the icons corresponding to a specified cell having a specified function corresponding to the specified icon.

[c15] 15. The integrated circuit design system of claim 2, wherein the logic unit is further capable of dividing the timing slack report into a plurality of timing slack sub-reports, each of the timing slack sub-reports having less

information than that of the timing slack report.

[c16] 16. The integrated circuit design system of claim 15, wherein the logic unit divides the timing slack report into the timing slack sub-reports according to circuit components referenced by the timing slack report.

[c17] 17. The integrated circuit design system of claim 15, wherein the logic unit divides the timing slack report into the timing slack sub-reports according to clocks referenced by the timing slack report.